UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,233	10/20/2003	Kia Seng Low	02 P 15173 US / INTECH 3.	4063

48154 7590 08/26/2005

SLATER & MATSIL LLP
17950 PRESTON ROAD
SUITE 1000
DALLAS, TX 75252

EXAMINER	
SARKAR, ASOK K	
ART UNIT	**PAPER NUMBER**
2891	

DATE MAILED: 08/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/689,233	LOW ET AL.	
	Examiner	Art Unit	
	Asok K. Sarkar	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,7-9 and 11-68* is/are pending in the application.

4a) Of the above claim(s) *17-52* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,7-9,11-16 and 53-68* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1, 2, 4, 7 – 9, 11 – 16 and 53 – 67 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

2. Claim 63 is objected to because of the following informalities: In line 2, following the word "includes" the word "to" should be deleted. Appropriate correction is required.

Claim 9 is objected to because of the following informalities: In line 12, following the phrase " ... said first layer of" the phrase "dielectric material" should be changed to "second dielectric material". Appropriate correction is required.

Drawings

3. The corrected drawings mentioned in the remarks filed August 2, 2005 to have been submitted are not received. The Applicant is requested to resubmit the corrected drawings for inclusion in the file.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 2, 8, 9, 11, 13,16, 53, 54, 57, 60, 61, 63, 64 and 68 are rejected under 35 U.S.C. 102(b) as being anticipated by Boeck, US 5,880,018.

Regarding claims 1, 13, 53, 60 and 63, Boeck teaches a method of incorporating

a first dielectric material into a layer of an electronic structure that includes at least one conductive line of a semiconductor device, said layer of electronic structure and said at least one conductive line being fabricated by a process that includes at least one thermal processing step at a temperature greater than a maximum withstand temperature of said dielectric material, said method comprising:

- fabricating said layer of electronic structure and said al least one conductive line 14 and 20 at least through the thermal processing step, said layer comprising a second dielectric material 20 formed atop an etch stop layer 16 and lying adjacent said at least one conductive line and said second dielectric material having a maximum withstand temperature greater than the temperature of the thermal processing step with reference to Fig. 3;
- removing at least a portion of said second dielectric material from said layer down to said etch stop layer with reference to Fig. 4 ; and
- depositing a layer of said first dielectric material 22 in place of the removed portion of said second dielectric material with reference to Fig. 5 in between column 3, line 10 and column 4, line 67.

Regarding claims 2, 11, 54, 61 and 64, Boeck teaches first dielectric material 22 has a lower dielectric constant than the second dielectric material in column 4, lines 45 – 67.

Regarding claims 8, 16, 57 and 68, Boeck teaches the step of depositing a layer of said first dielectric material includes depositing said layer atop said conductive line; and planarizing said layer of said first dielectric material such that a portion thereof

remains atop said conductive line and serves as an inter – level dielectric layer with reference to Fig. 6 and in column 4, lines 45 – 67.

Regarding claim 9, Boeck teaches a meemd of incorporating a first dielectric material into an insulator structure that is adjacent to at least one conductive line of a semiconductor device said insulator structure and said at least one conductive line being fabricated by a process that includes at least one thermal processing step at a temperature- greater than a maximum withstand temperature of said first dielectric material, said method comprising:

fabricating said insulator structure and said at least one conductive line at least through the thermal processing step using a second dielectric material that has a maximum withstand temperature greater than the temperature of the thermal processing step, said fabricating step comprising:

- depositing a first layer of said second dielectric material 12 atop a surface of a semiconductor substrate (see Fig. 1),
- planarizing said first layer of said second dielectric material 12 to a top-surface of another conductive line disposed atop said semiconductor substrate,
- depositing another layer of said second dielectric material 18 atop said first layer of said second dielectric material 12 and atop said another conductive line (see Fig. 1),
- patterning and etching said another layer of said second dielectric material to form at least one opening therein (see Fig. 2), and

- filling said opening with at least one conductive material 14 and 20 to form said at least one conductive line (see Fig. 3);
- removing at least a portion of said second dielectric material (see Fig. 4), and
- depositing a layer of said first dielectric material 22 in place of the removed portion of said second dielectric material.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 4, 12, 14, 55, 58, 62, 65 and 66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boeck, US 5,880,018.

Regarding these claims especially claim 58, Boeck teaches all limitations as were described earlier in rejecting claims 1, 53 and 60 and using contact barrier layer 49 in column 6, line 27 with reference to Fig. 10, but fails to teach annealing of the barrier layer at a temperature greater than the maximum withstand temperature of the first dielectric material.

However, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Boeck and anneal the barrier layer since annealing is conventional for the benefit of making the layer pinholes free for providing proper barrier function and the annealing temperature will also be greater than the maximum withstand temperature of the first dielectric material since the melting temperature of the low – k dielectric materials are quite low.

Regarding claims 14 and 66, Boeck fails to teach a timed etching step for the dielectric material.

However, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify the etching step by applying a timed etching to stop the etching at a time when the etching reaches the conductive plugs.

10. Claims 7, 15, 56, 59 and 67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boeck, US 5,880,018 in view of Seta, US 2002/0102843.

Regarding these claims, especially 59, Boeck teaches all limitations as were described earlier in rejecting claims 1, 53 and 60. Boeck also teaches planarizing the layer of first dielectric material to a top surface of the conductive line with reference to Fig. 6, and teaches that process steps can be repeated in order to form another sets of interconnects overlying one conductive interconnect to form multiple layer interconnects but fails to teach depositing another layer of the first dielectric material atop said layer of planarized dielectric material and atop said conductive line.

Seta teaches that a two layer interconnect can be formed by depositing another layer of the first dielectric material 116 atop the layer of planarized dielectric material 116and atop said conductive line 110 with reference to Fig. 34A for the benefit of forming interconnects with height differences in a two layer structure in paragraph 352.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Boeck and deposit another layer of the first dielectric material atop said layer of planarized dielectric material and atop said conductive line for the benefit of forming interconnects with height differences in a two layer structure as taught by Seta in paragraph 352.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 571 272 1970. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William B. Baumeister can be reached on 571 272 1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Asok K. Sarkar
August 24, 2005

Primary Examiner